

FUNCTION TABLE
(each latch)

INPUTS		OUTPUTS	
D	C	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant

Q_0 = the level of Q before the high-to-low transition of G

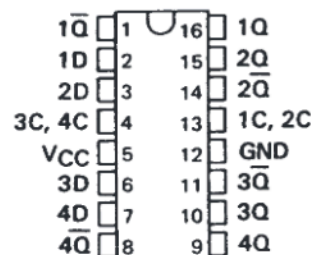
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

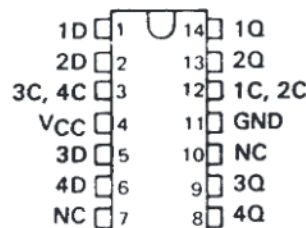
The '75 and 'LS75 feature complementary Q and $\bar{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, and 74LS devices are characterized for operation from 0°C to 70°C.

SN5475, SN54LS75 . . . J OR W PACKAGE
SN7475 . . . N PACKAGE
SN74LS75 . . . D OR N PACKAGE
(TOP VIEW)

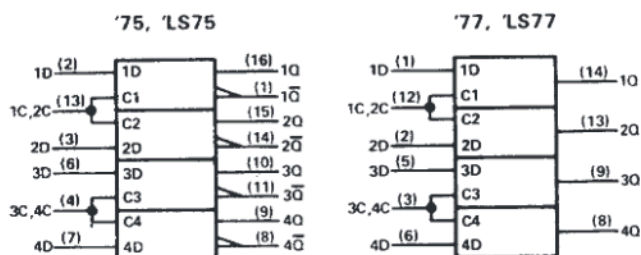


SN5477, SN54LS77 . . . W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage: '75, '77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

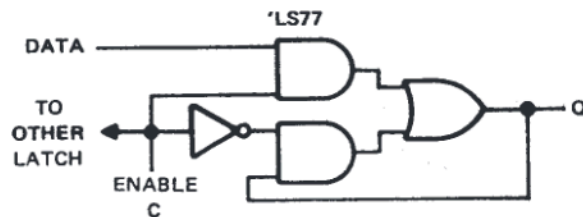
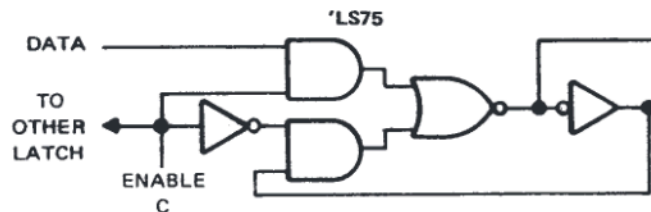
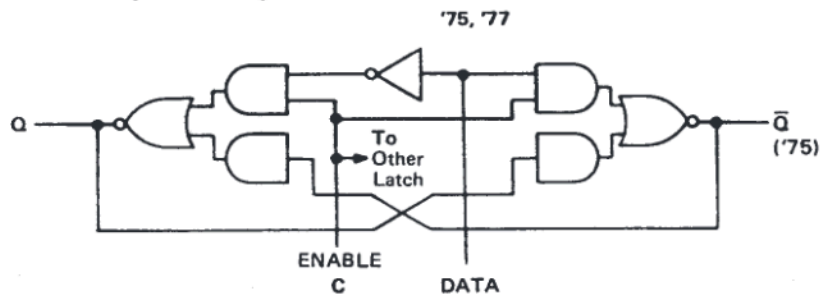
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

SN5475, SN5477, SN54LS75, SN54LS77 SN7475, SN74LS75

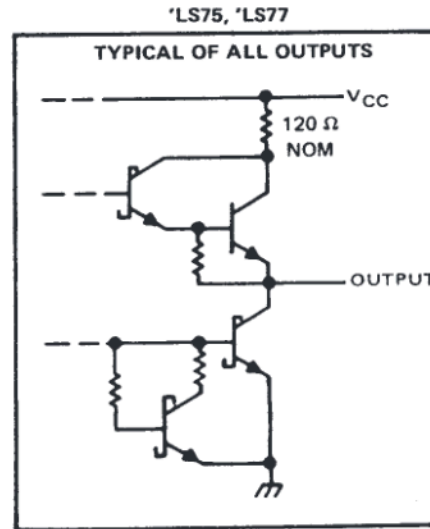
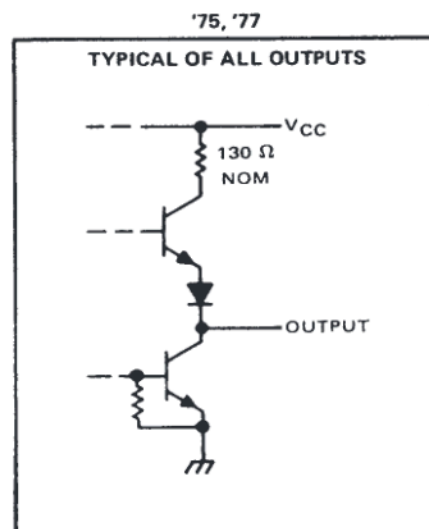
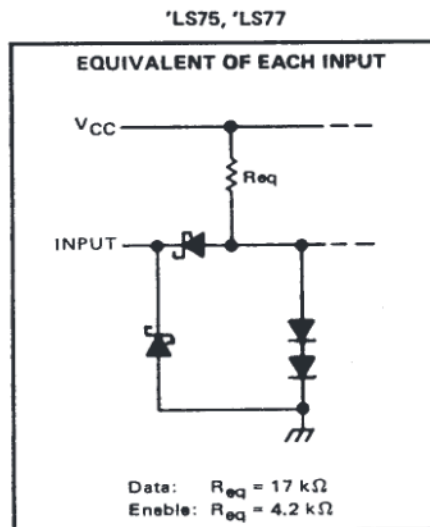
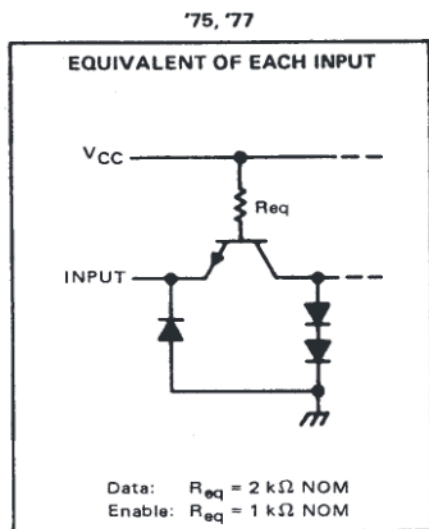
4-BIT BISTABLE LATCHES

SDLS120 – MARCH 1974 – REVISED MARCH 1988

logic diagrams (each latch) (positive logic)



schematics of inputs and outputs



SN5475, SN5477, SN54LS75, SN54LS77
SN7475, SN74LS75
4-BIT BISTABLE LATCHES

SDLS120 – MARCH 1974 – REVISED MARCH 1988

recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	D input	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			80	μ A
		C input				160	
I_{IL}	Low-level input current	D input	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-3.2	mA
		C input				-6.4	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54*	-20		-57	mA
			SN74*	-18		-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3	SN54*		32	46	mA
			SN74*		32	53	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	D	Q	C _L = 15 pF, R _L = 400 Ω, See Figure 1	16	30	ns	
t _{PHL}				14	25		
t _{PLH} ¶	D	Q̄		24	40	ns	
t _{PHL} ¶				7	15		
t _{PLH}	C	Q		16	30	ns	
t _{PHL}				7	15		
t _{PLH} ¶	C	Q̄		16	30	ns	
t _{PHL} ¶				7	15		

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

\P These parameters are not applicable for the SN5477.

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS75 SN54LS77			SN74LS75			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400 µA	2.5	3.5		2.7	3.5		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
							0.35	0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V	D input		0.1		0.1		mA
				C input		0.4		0.4		
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.7 V	D input		20		20		µA
				C input		80		80		
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V	D input		-0.4		-0.4		mA
				C input		-1.6		-1.6		
I _{OS}	Short-circuit output current§	V _{CC} = MAX		-20	-100		-20	-100		mA
I _{CC}	Supply current	V _{CC} = MAX,	See Note 2	'LS75	6.3	12	6.3	12		mA
				'LS77	6.9	13				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

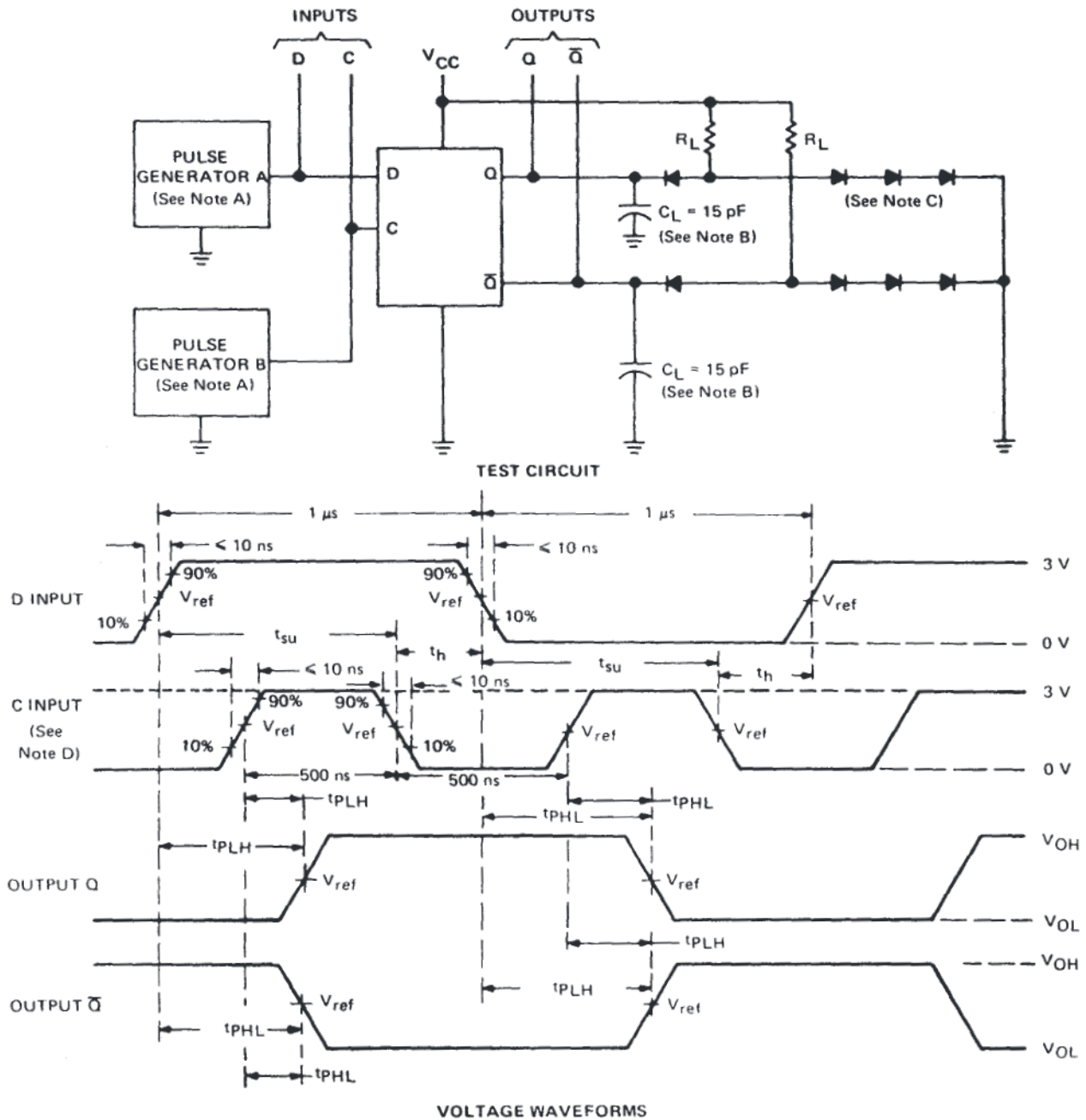
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	D	Q	CL = 15 pF, RL = 2 kΩ, See Figure 1	15	27		11	19	ns	
tPHL				9	17		9	17		
tPLH	D	Q̄		12	20				ns	
tPHL				7	15					
tPLH	C	Q		15	27		10	18	ns	
tPHL				14	25		10	18		
tPLH	C	Q̄		16	30				ns	
tPHL				7	15					

¶ t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation delay time, high-to-low-level output

switching characteristics†

PARAMETER MEASUREMENT INFORMATION



†Complementary Q outputs are on the '75 and 'LS75 only.

- NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$; for pulse generator A, $PRR \leq 500 \text{ kHz}$; for pulse generator B, $PRR \leq 1 \text{ MHz}$. Positions of D and C input pulses are varied with respect to each other to verify setup times.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. When measuring propagation delay times from the D input, the corresponding C input must be held high.
- E. For '75 and '77, $V_{ref} = 1.5 \text{ V}$; for 'LS75 and 'LS77, $V_{ref} = 1.3 \text{ V}$.

FIGURE 1

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