

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT259 8-bit addressable latch

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit addressable latch

74HC/HCT259

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices

capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.

The "259" also incorporates an active LOW common reset (\overline{MR}) for resetting all latches, as well as, an active LOW enable input (\overline{LE}).

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | | | |
| | D to Q_n | | 18 | 20 | ns |
| | A_n, \overline{LE} to Q_n | | 17 | 20 | ns |
| t_{PHL} | \overline{MR} to Q_n | | 15 | 20 | ns |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per latch | notes 1 and 2 | 19 | 19 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + \sum (C_L \cdot V_{CC}^2 \cdot f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \cdot V_{CC}^2 \cdot f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

8-bit addressable latch

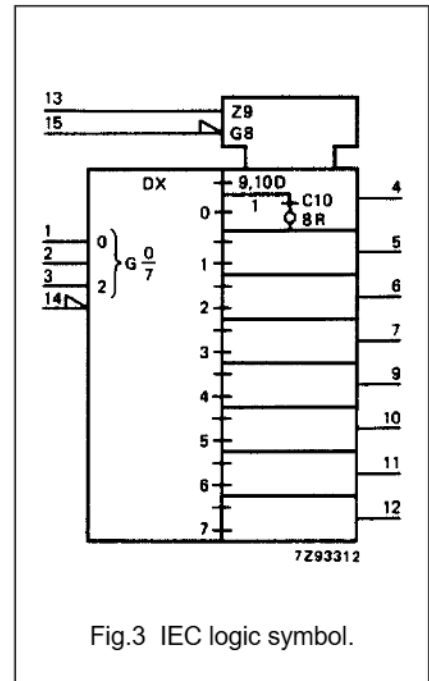
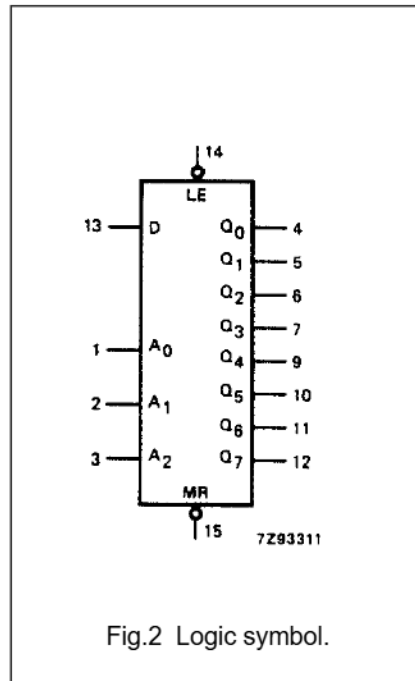
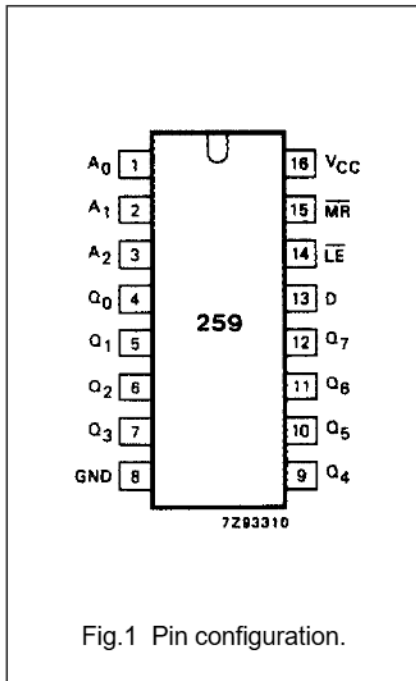
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ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

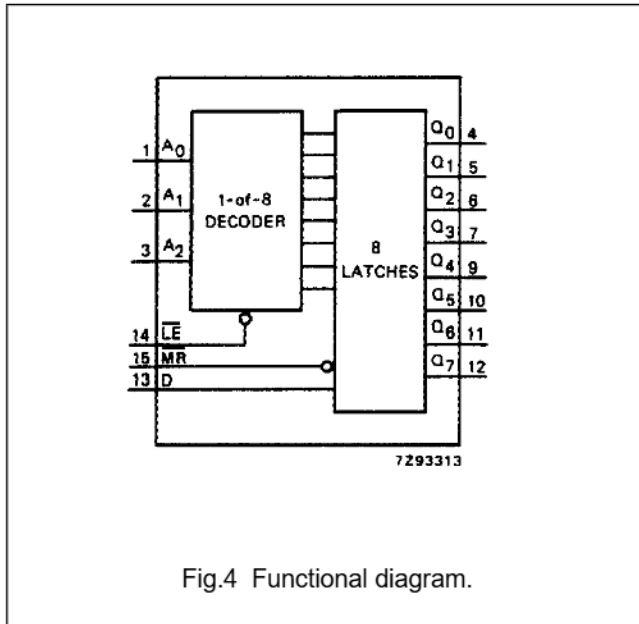
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---------------------------|----------------------------------|--------------------------------------|
| 1, 2, 3 | A ₀ to A ₂ | address inputs |
| 4, 5, 6, 7, 9, 10, 11, 12 | Q ₀ to Q ₇ | latch outputs |
| 8 | GND | ground (0 V) |
| 13 | D | data input |
| 14 | \overline{LE} | latch enable input (active LOW) |
| 15 | \overline{MR} | conditional reset input (active LOW) |
| 16 | V _{CC} | positive supply voltage |



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MODE SELECT TABLE

| $\overline{\text{LE}}$ | $\overline{\text{MR}}$ | MODE |
|------------------------|------------------------|-------------------------------------|
| L | H | addressable latch |
| H | H | memory |
| L | L | active HIGH 8-channel demultiplexer |
| H | L | reset |

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FUNCTION TABLE

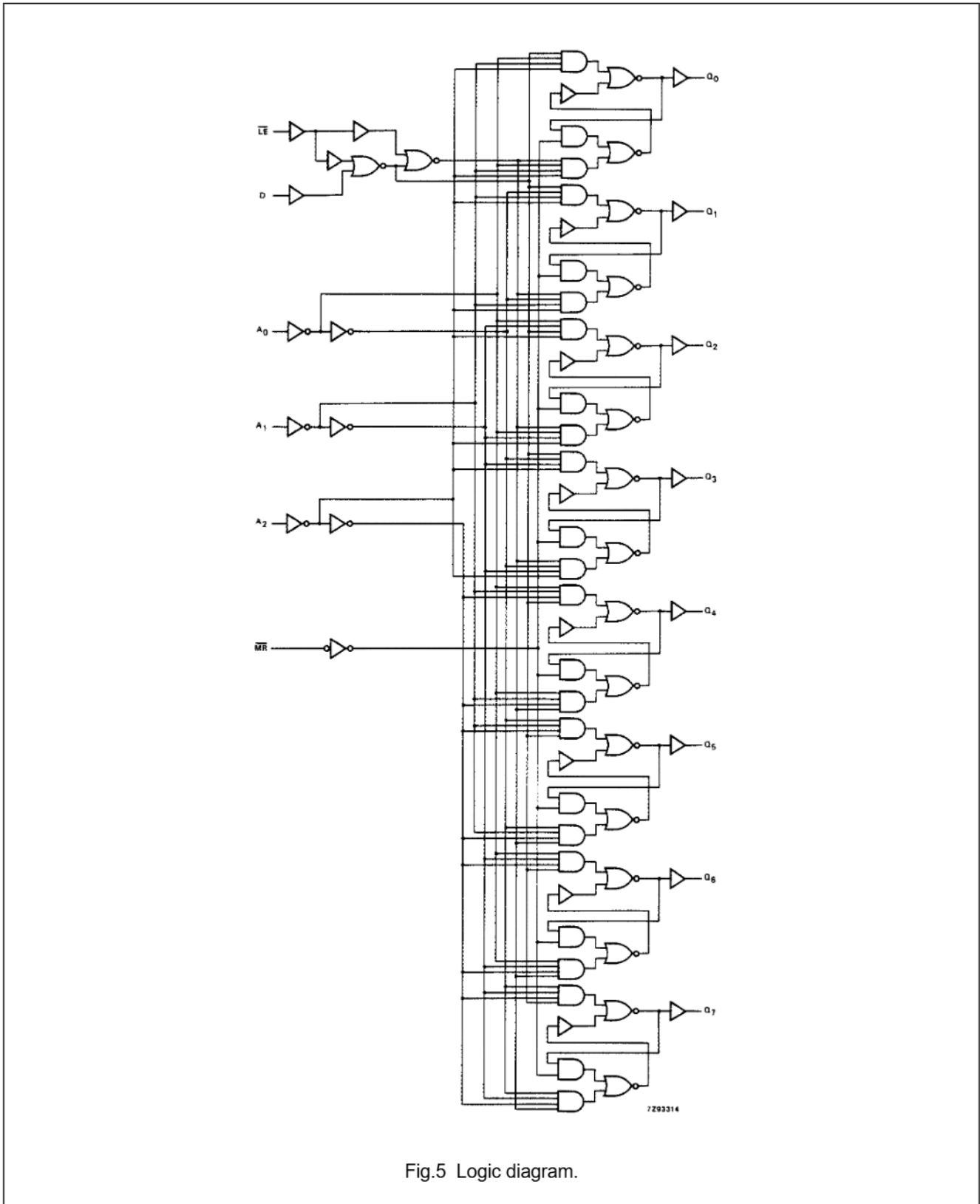
| OPERATING MODES | INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|------------------------|------------------------|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | $\overline{\text{MR}}$ | $\overline{\text{LE}}$ | D | A ₀ | A ₁ | A ₂ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q ₄ | Q ₅ | Q ₆ | Q ₇ |
| master reset | L | H | X | X | X | X | L | L | L | L | L | L | L | L |
| demultiplex (active HIGH) decoder (when D = H) | L | L | d | L | L | L | Q=d | L | L | L | L | L | L | L |
| | L | L | d | H | L | L | L | Q=d | L | L | L | L | L | L |
| | L | L | d | L | H | L | L | L | Q=d | L | L | L | L | L |
| | L | L | d | H | H | L | L | L | L | Q=d | L | L | L | L |
| | L | L | d | L | L | H | L | L | L | L | Q=d | L | L | L |
| | L | L | d | H | L | H | L | L | L | L | L | Q=d | L | L |
| | L | L | d | L | H | H | L | L | L | L | L | L | Q=d | L |
| | L | L | d | H | H | H | L | L | L | L | L | L | L | Q=d |
| store (do nothing) | H | H | X | X | X | X | q ₀ | q ₁ | q ₂ | q ₃ | q ₄ | q ₅ | q ₆ | q ₇ |
| addressable latch | H | L | d | L | L | L | Q=d | q ₁ | q ₂ | q ₃ | q ₄ | q ₅ | q ₆ | q ₇ |
| | H | L | d | H | L | L | q ₀ | Q=d | q ₂ | q ₃ | q ₄ | q ₅ | q ₆ | q ₇ |
| | H | L | d | L | H | L | q ₀ | q ₁ | Q=d | q ₃ | q ₄ | q ₅ | q ₆ | q ₇ |
| | H | L | d | H | H | L | q ₀ | q ₁ | q ₂ | Q=d | q ₄ | q ₅ | q ₆ | q ₇ |
| | H | L | d | L | L | H | q ₀ | q ₁ | q ₂ | q ₃ | Q=d | q ₅ | q ₆ | q ₇ |
| | H | L | d | H | L | H | q ₀ | q ₁ | q ₂ | q ₃ | q ₄ | Q=d | q ₆ | q ₇ |
| | H | L | d | L | H | H | q ₀ | q ₁ | q ₂ | q ₃ | q ₄ | q ₅ | Q=d | q ₇ |
| | H | L | d | H | H | H | q ₀ | q ₁ | q ₂ | q ₃ | q ₄ | q ₅ | q ₆ | Q=d |

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{\text{LE}}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|----------------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay D to Q _n | | 58 21 17 | 185 37 31 | | 230 46 39 | | 280 56 48 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay A _n to Q _n | | 58 21 17 | 185 37 31 | | 230 46 39 | | 280 56 48 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay $\overline{\text{LE}}$ to Q _n | | 55 20 16 | 170 34 29 | | 215 43 37 | | 255 51 43 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} | propagation delay $\overline{\text{MR}}$ to Q _n | | 50 18 14 | 155 31 26 | | 195 39 33 | | 235 47 40 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 119 22 19 | ns | 2.0 4.5 6.0 | Figs 6 and 7 |
| t _w | $\overline{\text{LE}}$ pulse width HIGH or LOW | 70 14 12 | 17 6 5 | | 90 18 15 | | 105 21 18 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _w | $\overline{\text{MR}}$ pulse width LOW | 70 14 12 | 17 6 5 | | 90 18 15 | | 105 21 18 | | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{su} | set-up time D, A _n to $\overline{\text{LE}}$ | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Figs 10 and 11 |
| t _h | hold time D to $\overline{\text{LE}}$ | 0 0 0 | -19 -6 -5 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _h | hold time A _n to $\overline{\text{LE}}$ | 2 2 2 | -11 -4 -3 | | 2 2 2 | | 2 2 2 | | ns | 2.0 4.5 6.0 | Fig.11 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| A _n | 1.50 |
| \overline{LE} | 1.50 |
| D | 1.20 |
| \overline{MR} | 0.75 |

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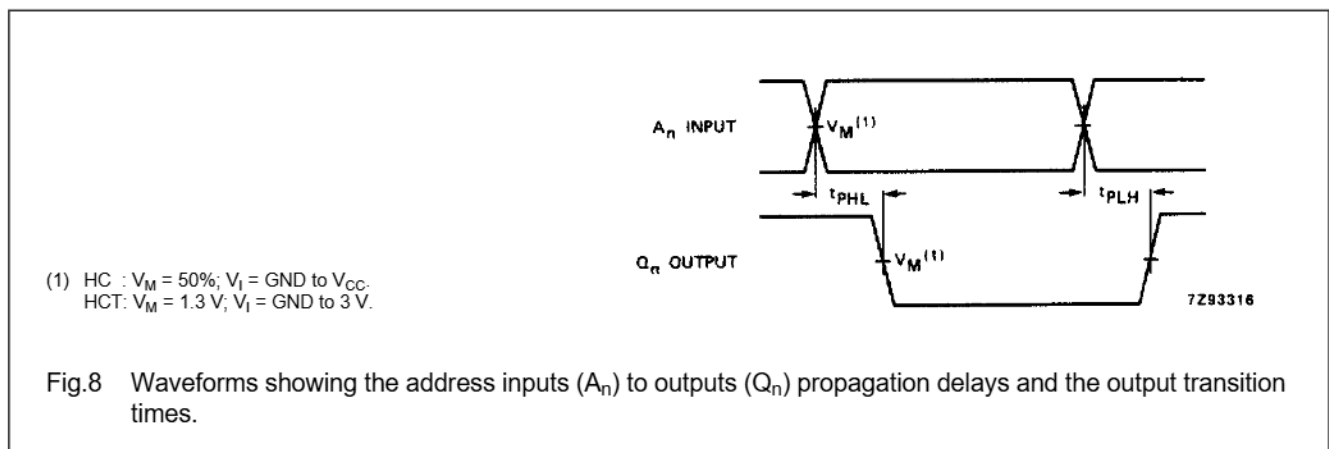
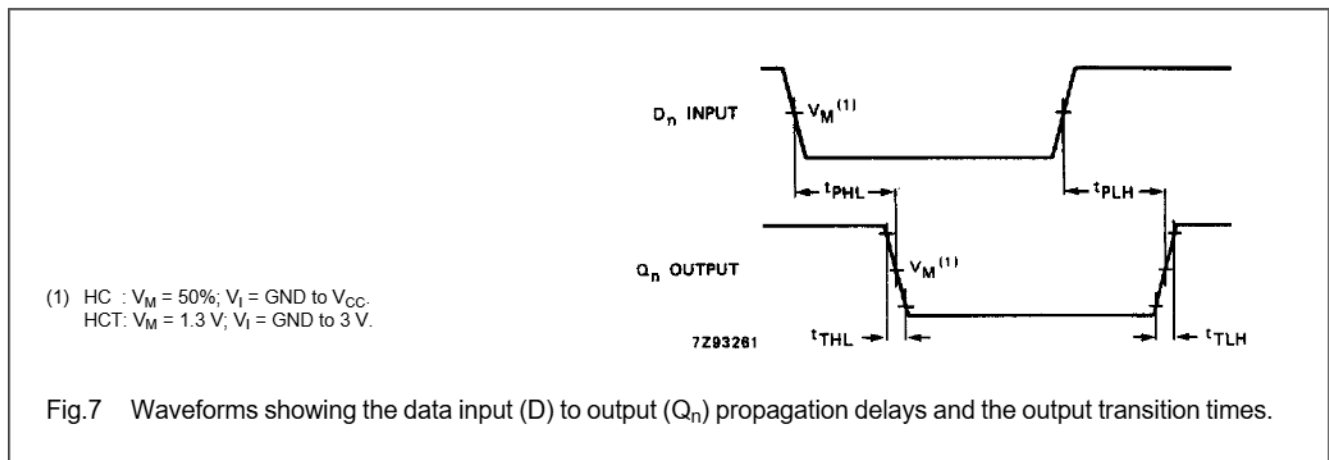
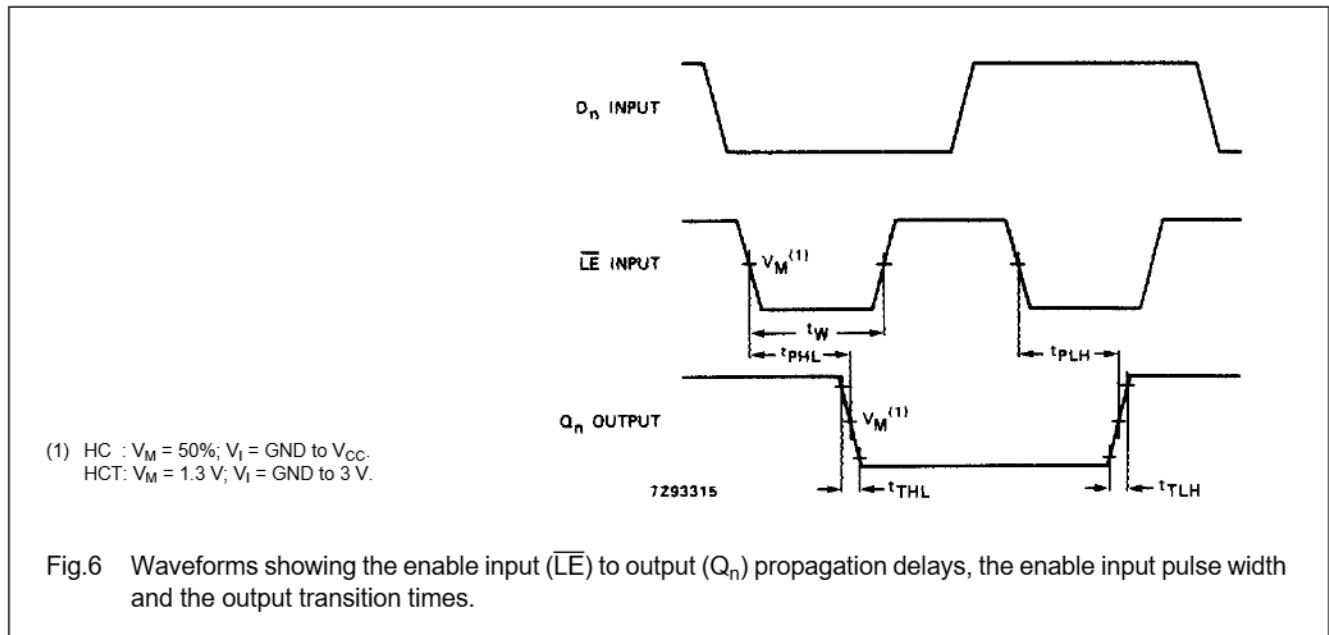
AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|---------------------|---|----------------|------|------|------------|------|-------------|------|----|------|-----------------|-----------|
| | | 74HCT | | | | | | | | | V_{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 TO +85 | | -40 TO +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t_{PHL} / t_{PLH} | propagation delay D to Q_n | | 23 | 39 | | 49 | | 59 | ns | 4.5 | Fig.7 | |
| t_{PHL} / t_{PLH} | propagation delay A_n to Q_n | | 25 | 41 | | 51 | | 62 | ns | 4.5 | Fig.8 | |
| t_{PHL} / t_{PLH} | propagation delay \overline{LE} to Q_n | | 22 | 38 | | 48 | | 57 | ns | 4.5 | Fig.6 | |
| t_{PHL} | propagation delay MR to Q_n | | 23 | 39 | | 49 | | 59 | ns | 4.5 | Fig.9 | |
| t_{THL} / t_{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Figs 6 and 7 | |
| t_W | \overline{LE} pulse width LOW | 19 | 11 | | 24 | | 29 | | ns | 4.5 | Fig.6 | |
| t_W | MR pulse width LOW | 18 | 10 | | 23 | | 27 | | ns | 4.5 | Fig.9 | |
| t_{su} | set-up time D to \overline{LE} | 17 | 10 | | 21 | | 26 | | ns | 4.5 | Fig.10 | |
| t_{su} | set-up time A_n to \overline{LE} | 17 | 10 | | 21 | | 26 | | ns | 4.5 | Fig.11 | |
| t_h | hold time D to \overline{LE} | 0 | -8 | | 0 | | 0 | | ns | 4.5 | Fig.10 | |
| t_h | hold time A_n to \overline{LE} | 0 | -4 | | 0 | | 0 | | ns | 4.5 | Fig.11 | |

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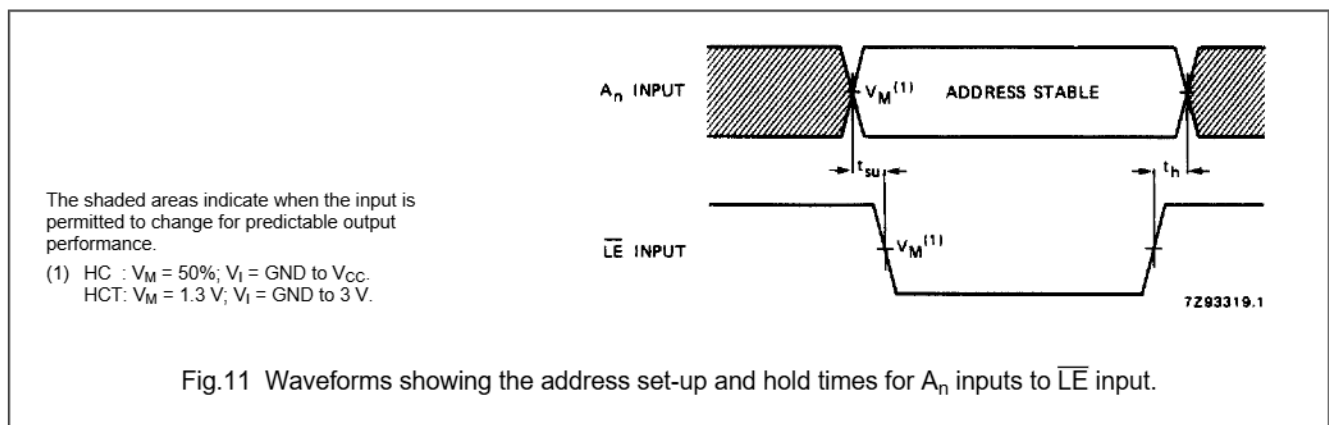
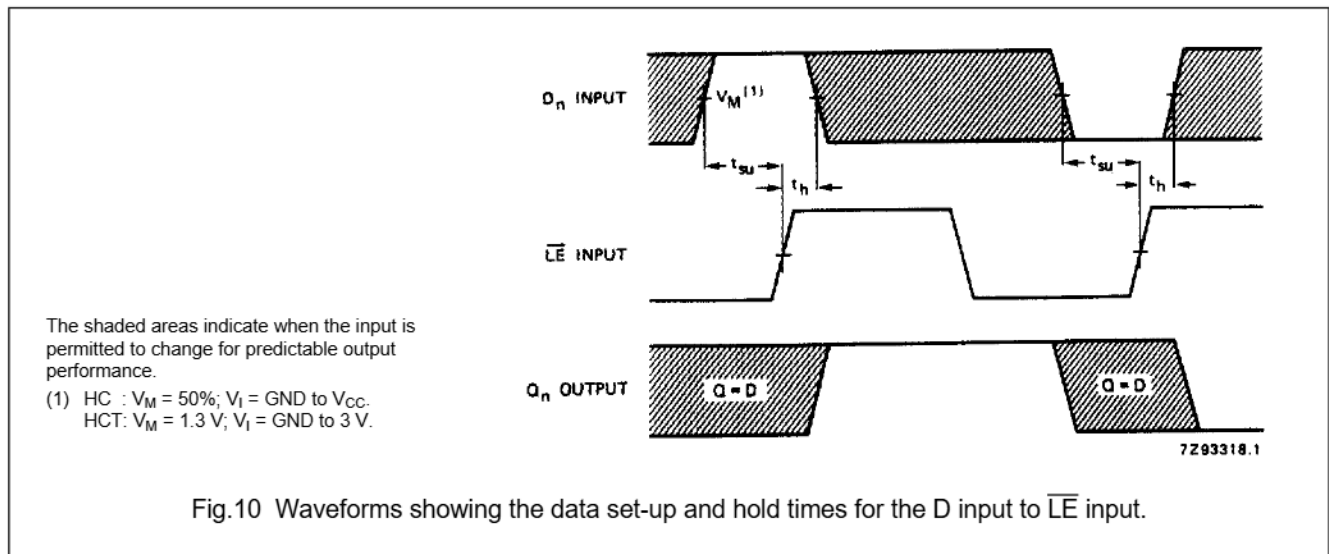
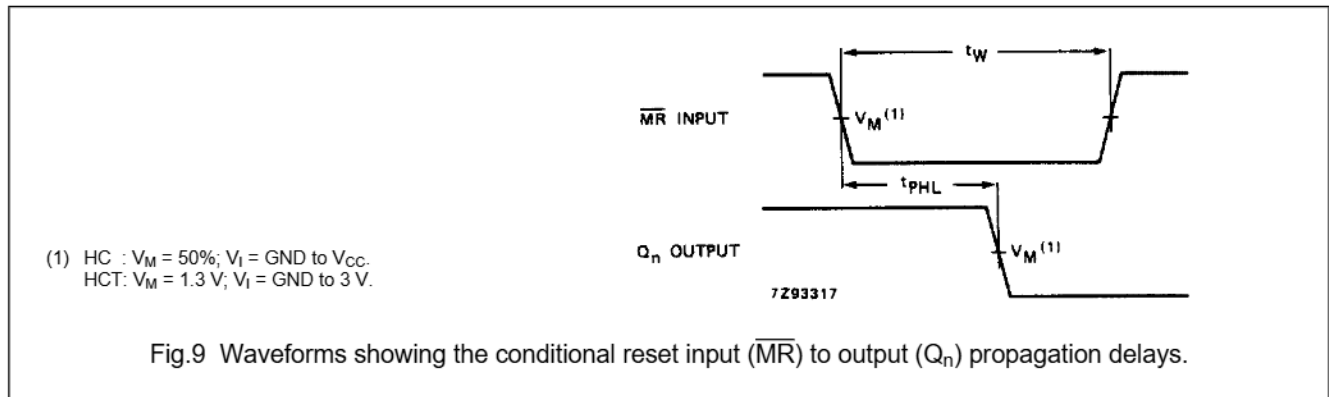
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AC WAVEFORMS



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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".