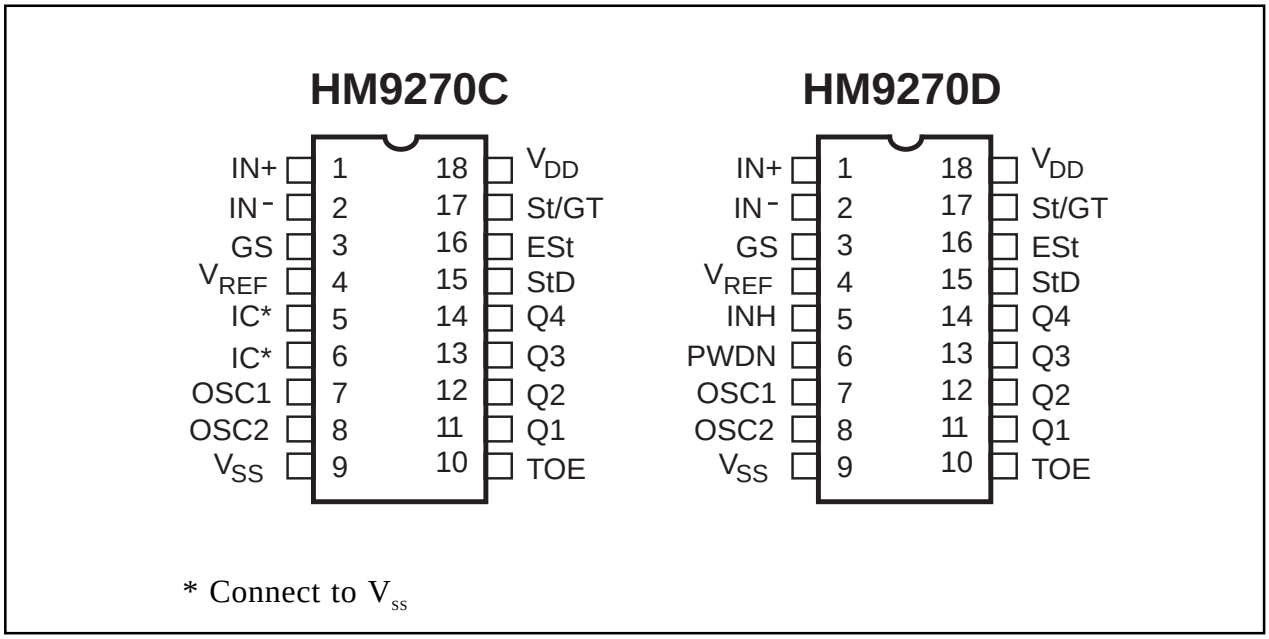
General Description

The HM 9270C/D is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high- and low-group filters and dial-tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock-oscillator and latched 3-state bus interface.

Features

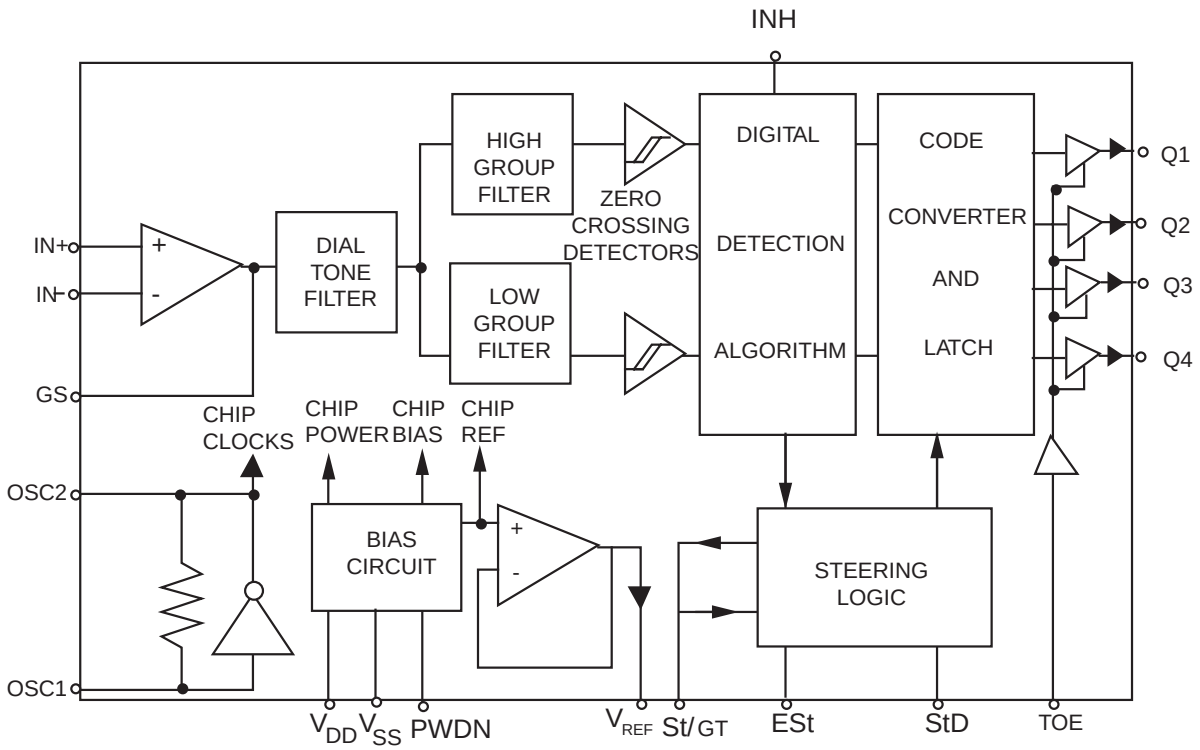
- Complete receiver in an 18-pin package.
- Excellent performance.
- CMOS, single 5 volt operation.
- Minimum board area.
- Central office quality.
- Low power consumption.
- Power-Down mode (HM9270D only).
- Inhibit-mode (HM9270D only).

Pin Configurations



* Connect to V_{ss}

Block Diagram (Figure 1)



Pin Description

Pin	Sym.	Function
1 2	IN+ IN-	Non-Inverting input Invering Input — Connections to the front-end differential amplifier.
3	GS	Gain select. Gives access to output of front-end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output,nominally $V_{DD}/2$. May be used to bias the inputs at midrail (see application diagram).
5	INH	Inhibit (input) logic high inhibit the detection of 1633Hz internal built-in pull down resistor. (HM9270D only).
6	PWDN	Power down (input). Active high power down the device and inhibit the oscillator internal built-in pull down resistor. (HM9270D only).
7 8	OSC1 OSC2	Clock Input Output — 3.579545 MHz crystal connected between these pins completes internal oscillator. Clock
9	V_{SS}	Negative power supply, normally connected to 0V.
10	TOE	3-state data output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.

Pin	Sym.	Function
11 12 13 14	Q1 Q2 Q3 Q4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see code table).
15	StD	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see truth table).
18	V_{DD}	Positive power supply, +5Volts.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Parameters	Min.	Max.	Units
Power Supply Voltage, V_{DD} - V_{SS}		6	V
Voltage on any pin	V_{SS} - 0.3	V_{DD}+ 0.3	V
Current at any pin		10	mA
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C
Package power dissipation		500	mW

Note 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating: -12 $^{mV}/_{oC}$ from 65°C to 85°C

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY:						
V_{DD}	Operating Supply Voltage		4.75		5.25	V
I_{cc}	Operating Supply Current			3.0	7	mA
P_o	Power Consumption	f=3.579MHz; V_{DD}=5V		15	35	mW
I_S	Standby Current	PWDN pin = V_{DD}	-	-	100	µA
INPUTS:						
V_{IL}	Low Level Input Voltage				1.5	V
V_{IH}	High Level Input Voltage		3.5			V
I_{IH}/I_{IL}	Input Leakage Current	V_{IN}=V_{ss} or V_{DD}		0.1		uA
I_{so}	Pull Up (Source) Current	TOE (Pin 10)=OV		7.5	15	uA
R_{IN}	Input Impedance Signal Inputs 1,2	@ 1kHz		10		MΩ
V_{TSt}	Steering Threshold Voltage			2.35		V

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
OUTPUTS:						
V_{OL}	Low Level Output Voltage	No Load		0.03		V
V_{OH}	High Level Output Voltage	No Load		4.97		V
I_{OL}	Output Low (Sink) Current	V_{OUT}=0.4V	1.0	2.5		mA
I_{OH}	Output High (Source) Current	V_{OUT}=4.6V	0.4	0.8		mA
V_{REF}	Output Voltage V_{REF}	No Load	2.4		2.7	V
R_{OR}	Output Resistance			10		KΩ

Operating Characteristics
Gain Setting Amplifier

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
I_{IN}	Input Leakage Current	$V_{SS} < V_{IN} < V_{DD}$		±100		nA
R_{IN}	Input Resistance			10		MΩ
V_{OS}	Input Offset Voltage			±25		mV
PSRR	Power Supply Rejection	1kHz		60		dB
CMRR	Common Mode Rejection	-3.0V <V_{IN}< 3.0V		60		dB
A_{VOL}	DC Open Loop Voltage Gain			65		dB
f_C	Open Loop Unity Gain Bandwidth			1.5		MHz
V_O	Output Voltage Swing	R_L³100KΩ to V_{SS}		4.5		V_{PP}
C_L	Tolerable capacitive load(GS)			100		pF
R_L	Tolerable resistive load(GS)			50		KΩ
V_{CM}	Common Mode Range	No Load		3.0		V_{PP}

Notes : 1.All voltages referenced to V_{DD} unless otherwise noted.
2.V_{DD}= 5.0V, V_{SS} = 0V, T_A = 25ºC .

AC Characteristics

All voltages referenced to V_{SS} unless otherwise noted. V_{DD}=5.0V, V_{SS}=0V, T_A = 25ºC, F_{CLK}=3.579545 MNz, using test circuit of figure 2.

Parameter	Description	Min.	Typ.	Max.	Units	Notes
SIGNAL COITIONS:						
	Valid Input Signal level (each tone signal):MIN			-40	dBm	1,2,3,5,6,9,11
				7.75	mV_{RMS}	1,2,3,5,6,9,11
	MAX	+1			dBm	1,2,3,5,6,9,11
		883			mV_{RMS}	
	Twist Accept Limit: Positive		10		dB	2,3,6,9,11
	Negative		10		dB	
	Freq. Deviation Accept Limit		±1.5%±2 Hz		Nom.	2,3,5,9,11
	Freq. Deviation Reject Limit	±3.5%			Nom.	2,3,5,11
	Third Tone Tolerance		-16			2,3,4,5,9,10,11
	Noise Tolerance		-12		dB	2,3,4,5,7,9,10,11
	Dial Tone Tolerance		+18		dB	2,3,4,5,8,9,10,11

Parameter	Description	Min.	Typ.	Max.	Units	Notes
TIMING:						
t_{DP}	Tone Present Detection Time	5	14	16	ms	Refer to Fig. 4
t_{DA}	Tone Absent Detection Time	0.5	4	8.5	ms	
t_{REC}	Tone Duration Accept			40	ms	
t_{REC}	Tone Duration Reject	20			ms	(User Adjustable)
t_{ID}	Interdigit Pause Accept			40	ms	Refer to "Guard Time 20
t_{DO}	Interdigit Pause Reject		ms	Adjustment"		
OUTPUTS:						
t_{PQ}	Propagation Delay (St to Q)		8	11	µs	TOE= V_{DD}
t_{PSED}	Propagation Delay (St to StD)		12		µs	
t_{QSED}	Output Data Set Up (Q to Std)		4.5		µs	
t_{PTE}	Propagation ENABLE		50	60	ns	R_L=10kΩ
t_{PTD}	Delay (TOE to Q) DISABLE		300		ns	C_L=50pf
CLOCK:						
f_{CLK}	Crystal/Clock Frequency	3.5759	3.5795	3.581	MHz	
C_{LO}	Clock Output (OSC2) Capacitive Load			30	pf	

Notes: 1.dBm = decibels above or below a reference power of 1mW into a 600 Ohm load.
2.Digit sequences consists of all 16 DTMF tones.
3.Tone duration = 40mS Tone pause = 40mS.
4.Nominal DTMF frequencies are used.
5.Both tones in the composite signal have an equal amplitude.
6.Tone pair is deviated by ±1.5% ±2Hz.
7.Bandwidth limited (3kHz) Gaussian Noise.
8.The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9.For an error rate of less than 1 in 10,000.
10.Referenced to the lowest level frequency component in DTMF signal.
11.Added A 0.1µf capacitor between V_{DD} and V_{SS}.

Function Description

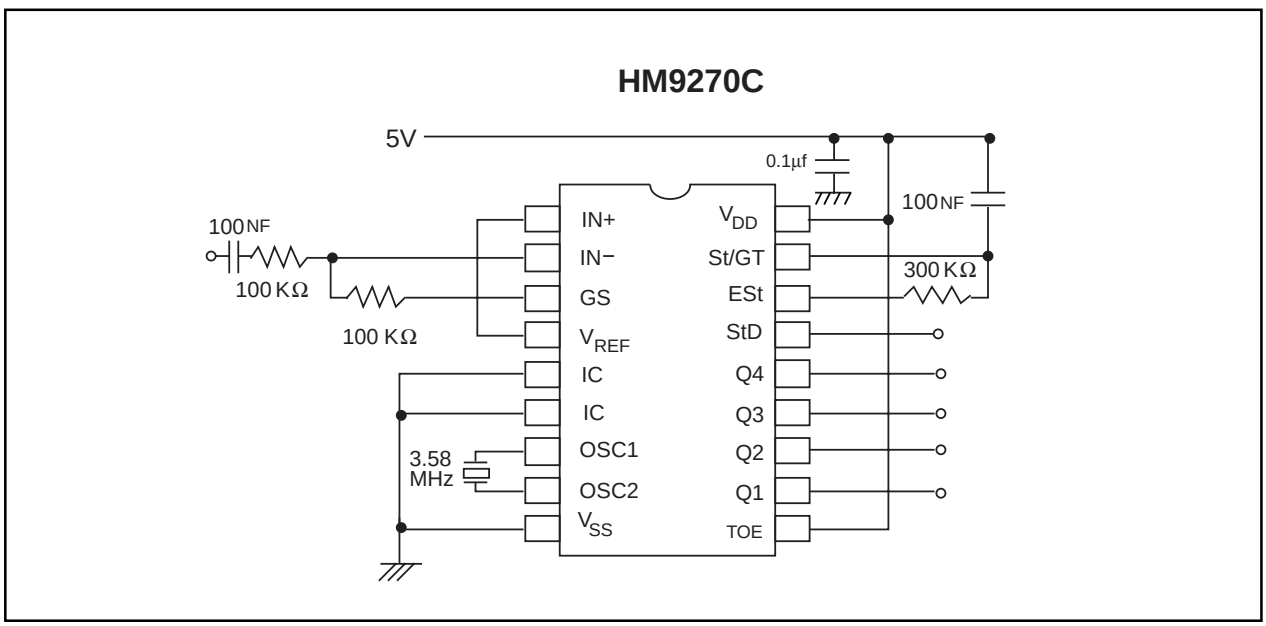


FIGURE 2. SINGLE ENDED INPUT CONFIGURATION

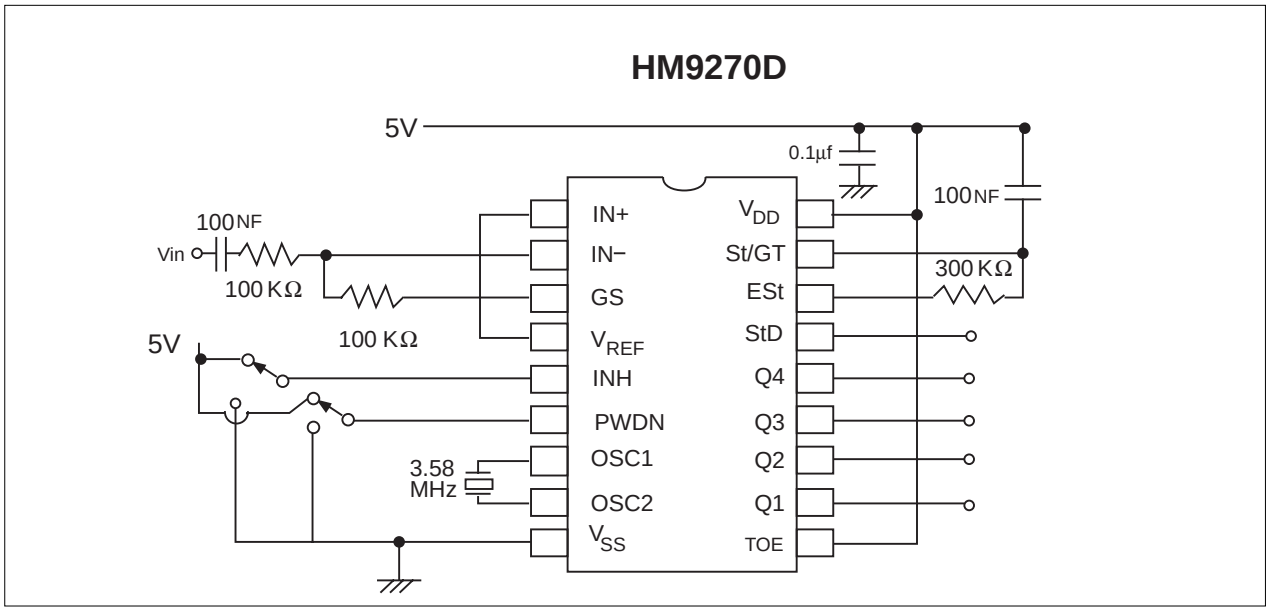


FIGURE 3. SINGLE ENDED INPUT CONFIGURATION

The HM9270C/D monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tones of receiver pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

FILTER SECTION

Separation of the low-group and high-group tones is achieved by applying the dual tone signal to the inputs of two filters a sixth order for the high group and an eighth order for the low group. The bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Fig. 4). The filter section also in corporates notches at 350Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second-order switched-capacitor section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

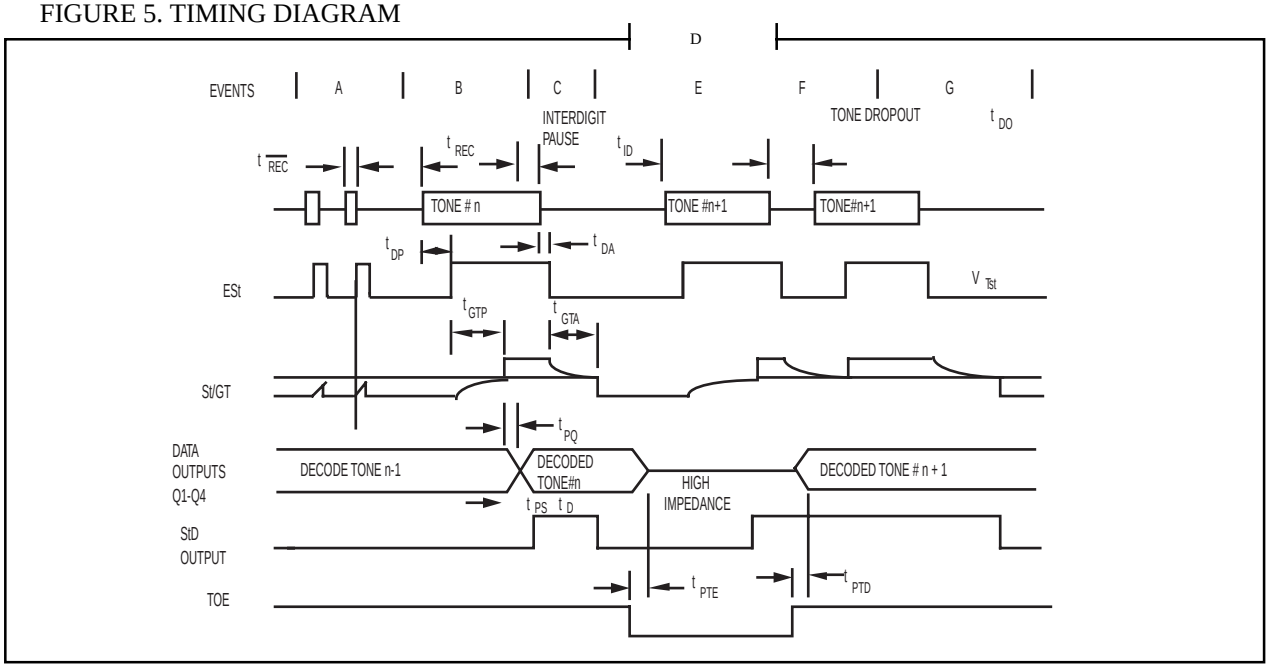
The decoder used digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm(protects) against tone simulation by extraneous signals, such as voice, while providing tolerance to smalll frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals ("third tones") and noise. When the detector recognizes the simultaneous presence of two valid tones (referred to as "signal condition" in some industry specifications), it raises the "early steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Flow	Fhigh	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW , H = LOGIC HIGH, Z = HIGH IMPEDANCE

FIGURE 4. LOGIC TABLE

FIGURE 5. TIMING DIAGRAM



A. Short tone bursts: detected. Tone duration is invalid.
B. Tone #n is detected. Tone duration is valid. Decoded to outputs.
C. End of tone #n is dectected and validated.
D. 3 State outputs disabled (high impedance).
E. Tone #n + 1 is detected. Tone duration is valid. De coded to outputs.
F. Tristate outputs are enabled. Acceptable drop out of tone #n + 1 does not negister at outputs.
G. End of tone #n + 1 is detected and validated.

FIGURE 5. TIMING DIAGRAM

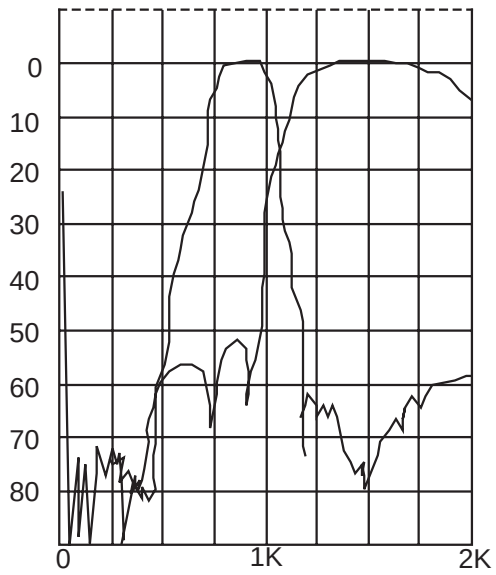


FIGURE 6. TYPICAL FILTER CHARACTERISTIC

STEERING CIRCUIT

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time-constant driven by ESt.

A logic high on ESt causes V_C (see Fig. 5) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone-pair, latching its corresponding 4-bit code (see Fig. 3) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally after a short delay to allow the output latch to settle, the "delayed-steering" output flag, StD, goes high, signaling that a recieved tone-pair has been registered. The contents of the output lacth are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit paues between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ("drop-out") too short to be considered a valid pause. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requiremetns.

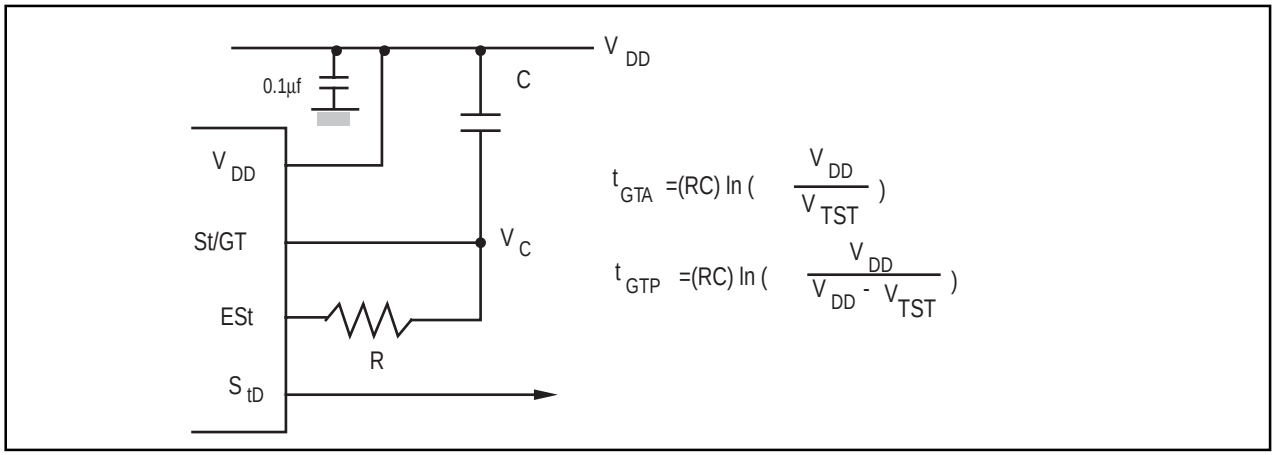


FIGURE 7. BASIC STEERING CIRCUIT

Guard Time Adjustment

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Fig. 7 is applicable. Component values are chosen according to the following formulae:

$t_{REC} = t_{DP} + t_{GTP}$ $t_{ID} = t_{DA} + t_{GTA}$

The value of t_{DP} is a parameter of the device (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40mS would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop - outs would be required. Design information for guard-time adjustment is shown in Fig. 8.

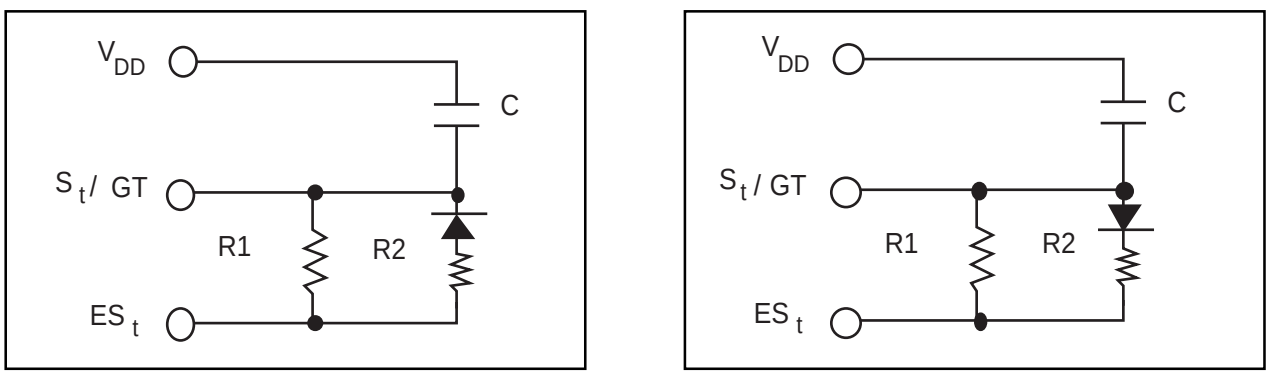


FIGURE 8. GUARD TIME ADJUSTMENT

Input Configuration

The input arrangement of the HM9270C/D provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.
Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.
In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{DD}$.
Fig. 9 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

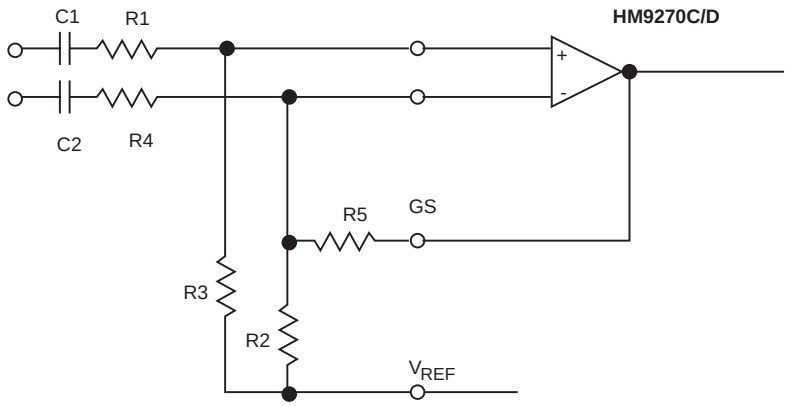


FIGURE 9. DIFFERENTIAL INPUT CONFIGURATION

Power - down and inhibit mode

A logic high applied to pin 6 (PWDN) will power the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.
Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of 1633 Hz. The output code will remain the same as the previous detected code (see table 1).

fLow	Fhigh	Key	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
-	-	ANY	L	Z	Z	Z	Z

fLow	Fhigh	Key	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	PREVIOUS DATA			
770	1633	B	H				
852	1633	C	H				
941	1633	D	H				
-	-	ANY	L	Z	Z	Z	Z

Table 1: Truth table

INH =V_{SS} (Z: high impedance) INH=V_{DD}

SPECIAL PACKAGE PIN CONFIGURATIONS

HM9270DM