

HD74LS74A

Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

REJ03D0415-0300 Rev.3.00 Jul.22.2005

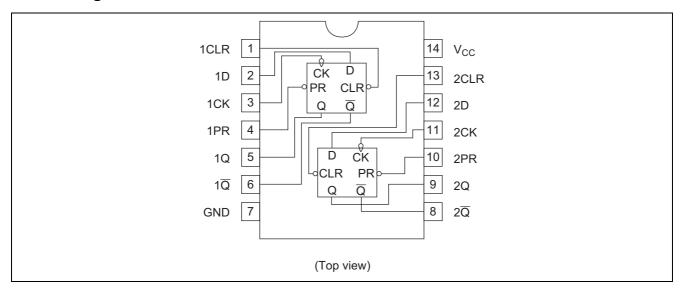
Features

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS74AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	Р	_
HD74LS74AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LS74ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

	Inp	Output			
Preset	Clear	Clock	D	Q	Q
L	Н	X	X	Н	L
Н	L	X	X	L	Н
L	L	X	X	H*	H*
Н	Н	↑	Н	Н	L
Н	Н	↑	L	L	Н
Н	Н	L	X	Q_0	\overline{Q}_0

H; high level, L; low level, X; irrelevant, ↑; transition from low to high level,

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Тур	Max	Unit		
Supply voltage		V _{CC}	4.75	5.00	5.25	V		
Outract company		Output ourrant		I _{OH}	_	_	-400	μΑ
Output current		I _{OL}	_	_	8	mA		
Operating temperature		Topr	-20	25	75	°C		
Clock frequency	y f _{clock}		0	_	25	MHz		
Pulse width	Clock High	t _w	25	_	_	no		
Fuise width	Clear Preset	t _w	25	_	_	ns		
Catua tima	"H" Data	t _{su}	20↑	_	_			
Setup time	"L" Data	t _{su}	20↑	_	_	ns		
Hold time		t _h	5↑	_	_	ns		

Note: ↑; The arrow indicates the rising edge.

Q₀; level of Q before the indicated steady-state input conditions were established.

 $[\]overline{Q}_0$; complement of \overline{Q}_0 or level of Q before the indicated steady-state input conditions were established.

^{*;}This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

Ite	em	Symbol	min.	typ.*	max.	Unit	Condition		
Input volto	Input voltage		2.0	_	_	V			
input voita	ige	V _{IL}	_	_	0.8	V			
		V _{OH}	2.7			V	$V_{CC} = 4.75 \; V, \; V_{IH} = 2 \; V, \; V_{IL} = 0.8 \; V, \\ I_{OH} = -400 \; \mu A$		
Output vol	lage	V	_	_	0.5	V	$I_{OL} = 8 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V},$		
		V _{OL}	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{IH} = 2 \text{ V}$		
	D		_	_	20				
	Clear] ,	_	_	40		V 525 V V 2.7 V		
	Preset	I _{IH}	_	_	40	μΑ	$V_{CC} = 5.25 \text{ V}, V_I = 2.7 \text{ V}$		
	Clock		_	_	20				
	D	I _{IL}	_	_	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V		
Input	Clear		_	_	-0.8				
current	Preset		_	_	-0.8				
	Clock		_	_	-0.4				
	D		_	_	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V		
	Clear] ,	_	_	0.2				
	Preset	l _l	_	_	0.2				
	Clock		_	_	0.1				
Short-circu	uit output	los	-20	_	-100	mA	V _{CC} = 5.25 V		
Supply cu	rrent	I _{CC} **	_	4	8	mA	V _{CC} = 5.25 V		
Input clam	p voltage	V_{IR}		_	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA		

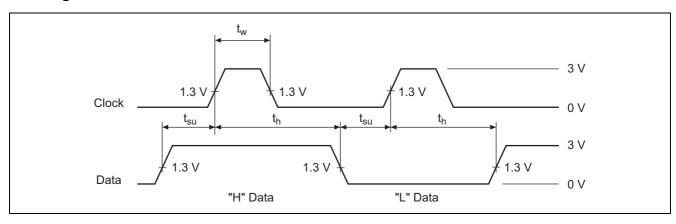
Notes: $^*V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}$

Switching Characteristics

$$(V_{CC} = 5 \text{ V}, \text{Ta} = 25^{\circ}\text{C})$$

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}			25	33		MHz	C _ 15 pE
Propagation delay time	t _{PLH}	Clear, Clock	Q, \overline{Q}	_	13	25	ns	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$
Fropagation delay time	t _{PHL}	or Preset		_	25	40	ns	NL - 2 N22

Timing Definition

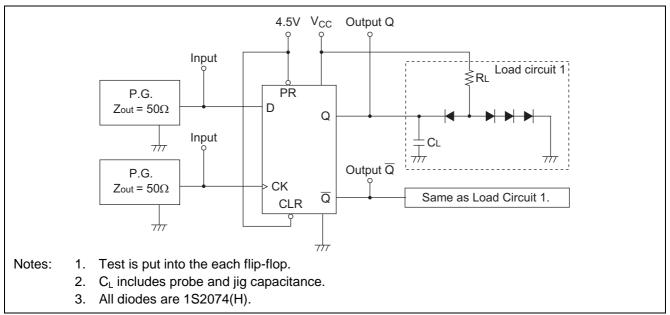


^{**} With all output open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

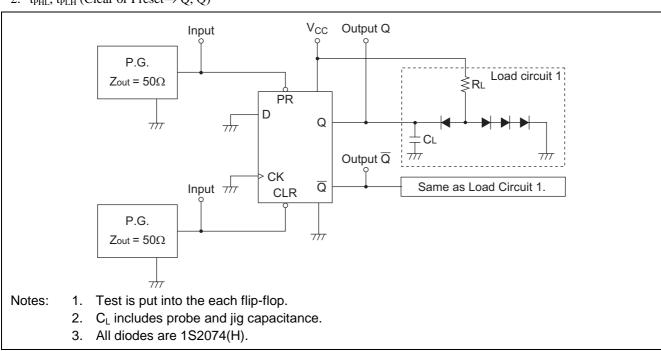
Testing Method

Test Circuit

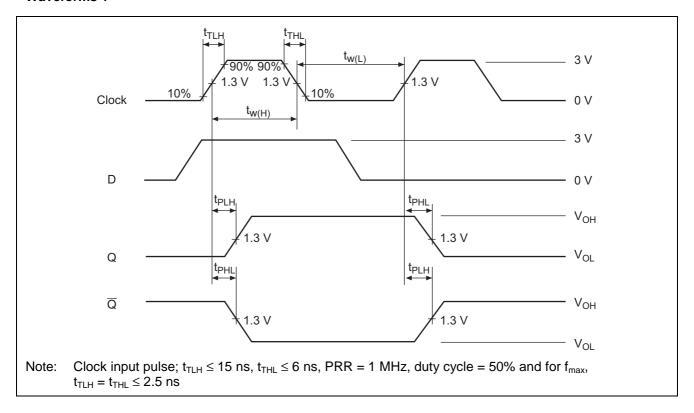
1. f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \overline{Q})



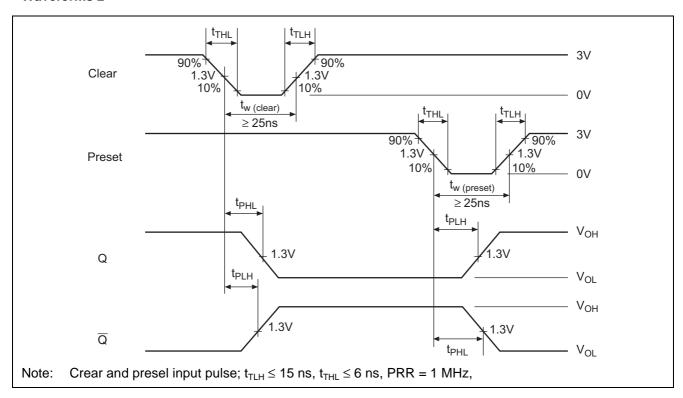
2. t_{PHL} , t_{PLH} (Clear or Preset \rightarrow Q, \overline{Q})



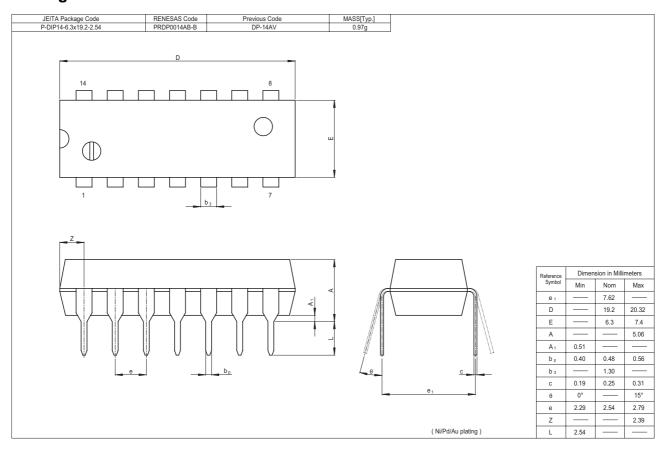
Waveforms 1

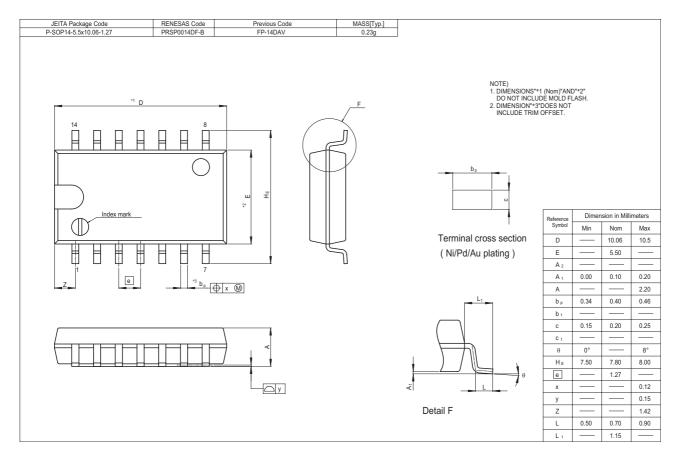


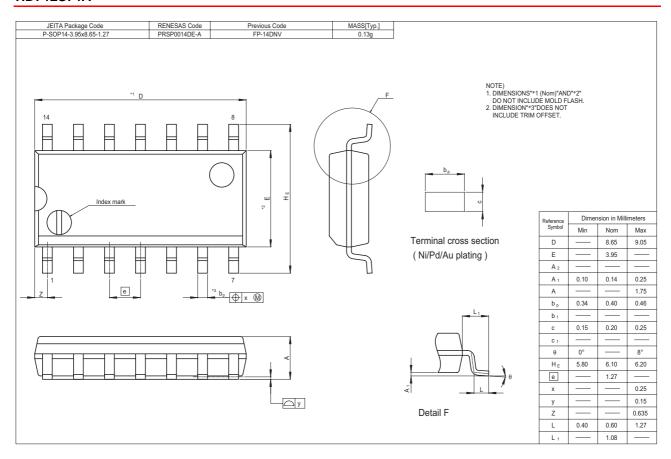
Waveforms 2



Package Dimensions







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